Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **VCC+**
2. **IN+**
3. **IN-**
4. **VCC-**
5. **LATCH ENABLE**
6. **GND**
7. **Q OUT**
8. **NOT Q OUT**

**.063”**

**.055”**

**1 1 8**

**1**

**2**

**3**

**7**

**6**

**6**

**6**

**4 5**

**TL3016**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: FLOATING**

**Mask Ref: TL3016**

**APPROVED BY: DK DIE SIZE .055” X .063” DATE: 4/27/23**

**MFG: TEXAS INSTRUMENTS THICKNESS .013” P/N: TL3016Y**

**DG 10.1.2**

#### Rev B, 7/1